Efficient QPSK Burst Demodulator for Onboard Application

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Abstract-**This paper analyzes and presents simulation and experimental results for a hardware implementation of a low-overhead digital coherent burst demodulator for onboard signaling channel systems using short bursts. This implementation is based on digitizing a received signal after a low-frequency IF conversion, AGC and performing all demodulation functions using digital signal processing (DSP) techniques. Demodulation with very low overhead is made possible by storing a burst in memory. A novel feed forward loop preambleless structure performs carrier recovery. Symbol-timing and carrier frequency-offset estimations are performed by block processes using the error signal resulting from differential demodulation.**
Keywords: BER, Eb/No, IFIR, UW, FEC, DDPLL.

I. INTRODUCTION

The typical packet format used for burst communications and signaling in a time division multiple access (TDMA) network employs a structure that includes an acquisition preamble at the start of the packet, followed by a known unique word (UW) pattern. The data portion of the packet then follows with additional framing bits inserted periodically for long packets, with the packet finally ending in another known "end-of-packet" sequence. The preamble portion typically incorporates an unmodulated carrier sequence for faster carrier frequency and phase estimation at the receiver, followed by a clock recovery sequence for the proper receiver clock frequency and phase alignment. The unique word pattern is used for the phase ambiguity resolution and burst time synchronization. Thus, after the preamble and *UW* segments have been received and detected upon, the receiver is ready to demodulate the ensuing data segment with the correct frequency, phase, and clock adjustments. Fig.-1.a shows the packet format of the burst demodulator.

In practice, however, the required preamble that precedes the data portion of the packet often constitutes an excessive overhead (fig 1.a) that reduces the channel transmission efficiencies for short data packets. Particularly for the case of mobile and maritime communication networks that experience signal fades of varying degrees, the system design mandates the use of very short data bursts relatively immune to fades (-a few hundred

bits). These bursts are generally used for the channel request and assignment functions from the remote terminal to a central location, typically a network coordination center. With additional channel impairments such as Doppler shifts, low carrier-to-noise ratios, and frequency offsets, long acquisition preambles are usually required to correctly locate the carrier and acquire its frequency and phase. The use of a long preamble in this case is an extremely undesirable overhead that seriously undermines the channel transmission efficiencies for a large communication network with potentially thousands of such remote terminals.

So the preamble-less burst demodulator is a novel approach which does not have a preceding preamble and the overheads are reduced. These bursts are generally used for the channel request and transmission purpose. The use of a long preamble is an extremely undesirable overhead that seriously undermines the channel transmission efficiencies for a large communication network with thousands of potential terminals. Hence, the design and simulation of this preamble-less burst demodulator is done and discussed here.

Fig.-1.b shows the packet format of the preamble-less burst demodulator. The Carrier Recovery and BTR bits are not present in this and the packet begins with the Unique Word bits. The challenge in this is to acquire the carrier frequency from the modulated data bits in a limited time period and the burst needs to be stored in the buffer first and then processed for the acquisition of carrier initially and then the unique word pattern to mark the beginning of data.
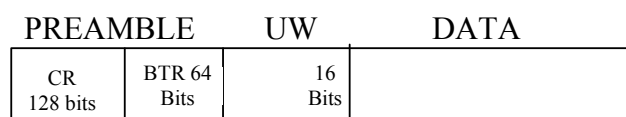
PREAMBLE		UW	DATA
CR 128 bits	BTR 64 Bits	16 Bits	

Fig.-1.a Packet Format Of Conventional Burst Demodulator
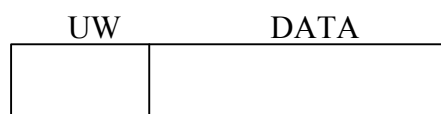
UW	DATA

Fig.-1.b Packet Format Of Preamble-less Burst Demodulator

This paper presents the generalized efficient acquisition algorithms, and the hardware and software solutions for a compact, low cost, all-digital burst demodulator that requires absolutely no acquisition preamble. Both the acquisition algorithms and the hardware architecture are selected to be applicable for a wide variety of system constraints, and are particularly well suited for the reception of short data packets under very adverse channel conditions.

II. SPECIFICATIONS

The Table-1 gives overall specifications of the demodulator. The Table-2 gives the specifications used for the hardware platform. The Table-3 gives the specifications used for the implementation of algorithm based on digital signal processing techniques.

TABLE I.   Overall Specifications of demodulator

Transmission data rate	2.048 Mbps
Input IF signal frequency	70 Mhz
Modulation	QPSK ½ FEC
Mode	Burst
Phase ambiguity resolution	By differential encoding and decoding
Decision	Hard decision
Output interface	TTL
BER	$1*10^{-7}$ at 9 dB Eb/No

TABLE II.   Hardware Requirments

Processor	Analog Device chip ADSP-21020 (Radiation hardened)
Clock Speed	36.864 Mhz
Data SRAM Program SRAM	512k x 40 512k x 48
PROM	32k x 48
ADC	8-bit
Pre-filter	Analog, 3.072 MHz bandwidth
Power-supply	+5V,-5V

TABLE III.   Software Specifications

Processing mode	Block-by-block
Block length	18 bits
Mixer LO frequency	8.56 Mhz+Offset corrected frequency
Mixer output frequency	12.288 Mhz
Samples/bit at input	12
ADC Sampling rate	49.152 Mhz
Samples/bit at IFIR heterodyne output	3
Timing offset	6
Integration time for phase error estimate	36 bits
Time require for Carrier acquisition and Bit timing recovery	50ms
Unique word detection time	40ms
Complete Data demodulation	120 ms
Minimum Burst to Burst gap	350 ms

III. STRUCTURE OF DEMODULATOR

The structure of the demodulator [2] is described in figure – 2.The input QPSK modulated signal at 70 Mhz is passed through an analog filter of 3.072 Mhz bandwidth. Then the signal is amplified for ±1 V peak-to-peak level before giving to S/H for sampling. The S/H circuit is clocked by a

Actel FPGA , which is controlled by DSP to sample at the required sampling rate. The S/H output is quanitized by an ADC for 8-bit resolution.

The samples are digitally processed by ADSP-21020. The samples are collected for 18 bits and stored in switching dual-buffer on continuous basis. The DSP processes the samples of a buffer and demodulates the data before the other buffer is filled fully.The input samples of a block are
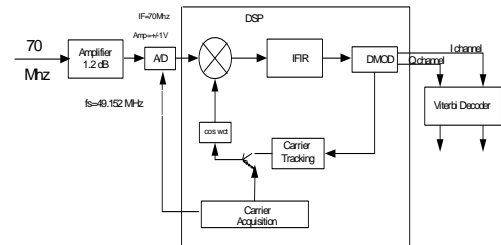

Fig. 2. Overall Block Diagram of Demodulator

first mixed with LO. The output of mixer is passed through Interpolated FIR filter and decimated to recover baseband data. The output of IFIR is subjected to matched filtering for clock recovery and decision.

The raw I and Q channel data is integrated for phase error estimation over block length. This is used to correct the LO frequency for carrier tracking. The demodulator also implements carrier recovery to estimate the carrier frequency with sufficient accuracy at starting for locking.

IV. SOFTWARE STRUCTURE

The software flow of the demodulator using digital signal processing techniques [3] is described in figure – 3.
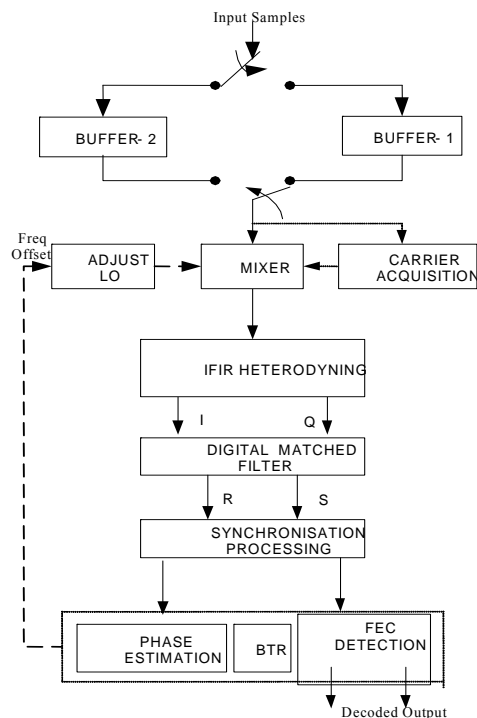

Fig. 3 Software Block Schematic of Demodulator

As shown in the figure 3 , the samples of the input signal are acquired in two buffers and passed through the mixer to obtain the signal at lower IF for further processing. The samples at the output of the mixer are passed through the IFIR (Interpolated FIR) heterodyning stage to obtain the baseband I and Q data streams. Digital matched filtering is done on these baseband signals. Its purpose is to increase the signal component and reduce the noise component at the same time thus maximizing the signal to noise ratio at the output at some instant. This is followed by synchronisation processing which involves baud synchronisation, phase estimation, coherent detection and differential decoding. Block phase estimator helps in frequency tracking and the frequency offset correction is applied for the next block of data soft local oscillator.

The demodulator here requires an initial carrier reference during start and this is obtained from the carrier acquisition module. It makes the required correction to the local oscillator of the mixer.

V. MAJOR MODULES

The sampling frequency is 49.152 Mhz and the main program sets this frequency. There are 12 samples per bit and actual demodulation is done on block by block basis where each block is of 18 bits.

A Acquiring Data Samples

The main function of data acquisition routine is to capture the data from dual port RAM convert it into 32 bit floating point number and store back to SRAM for further processing. The data acquisition will begin only after initialization of hardware interrupt in main initialization module. To avoid data loss both dual port memory will be filled in ping-pong mode. This continuous data is further processed for carrier acquisition and data demodulation.

B Carrier acquisition

The main function of carrier acquisition routine is to detect carrier and to estimate exact frequency offset of the received burst. In the proposed demodulation method, the received burst signal is demodulated quasi-coherently and digitized, and stored in the buffer memory. Carrier and bit timing synchronizations are performed for the burst signal stored in the buffer memory. A large frequency offset is estimated by processing in frequency domain. Thereafter, a novel phase synchronizer copes with a short-term frequency variation. Fig: 4 shows the block diagram of the carrier acquisition module. It consists two components.

    i) Coarse carrier acquisition.
    ii) Fine frequency acquisition.

i). Coarse carrier acquisition

Since LPFl should have a broad bandwidth compared with the modulated carrier to allow a possible large frequency offset, the received signal contains excess noise and the succeeding signal processing will be taken under the condition of a very low signal to noise power ratio. In order to overcome the adverse effect of noise to a large extent ,the noise component in the received signal is reduced by "first frequency estimation " as shown in fig .4.
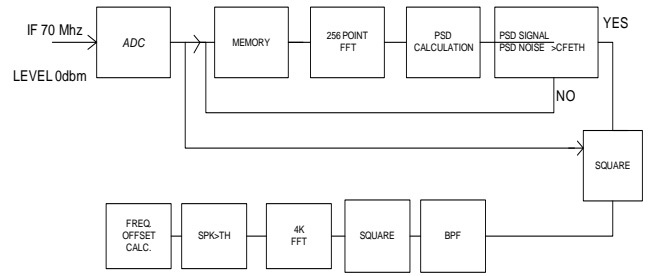

Figure.-4. Block Diagram Of Carrier Acquisition

In the first frequency estimator, the signal is transformed into the frequency domain by the first FFT(FFT 256 Point). In order to estimate the coarse center frequency, the modulated power spectra are searched throughout the range of the frequency offset expected in the received signal.

If the received noise is assumed to be a white Gaussian noise, the power density of the noise will be approximately constant over the frequency range of LPF1. On the other hand, the power spectrum of the modulated signal may have a higher level than the noise in the frequency range over the modulated signal bandwidth. With having recourse to this fact, the energy within a certain frequency window is calculated and the window **is** swept over the frequency offset range to obtain the coarse center frequency of the modulated signal as the center frequency of the window which have the maximum energy. Through this estimation, the coarse center frequency of the received signal is acquired and there is still a smaller frequency error in the signal at the output of LPF2.

ii). Fine frequency acquisition

The spectrum of QPSK modulated signal as shown in fig 5.a.Due to the first frequency estimation and LPF2, the noise component of the received signal is significantly reduced. Subsequently, this signal is fed to the complex squarer to extract the carrier component. The output of complex squarer is again fed to a Band pass filter whose centre frequency is double the carrier frequency. The band pass filter is required to remove extra noise due to non linear squaring operation. The filter output again fed to the second complex squarer in order to remove modulation completely. The output signal of the second squarer is transformed to the frequency domain by FFT2 (4K point).

In the absence of any frequency Variation during the burst duration, the frequency of the exact carrier component would be estimated because there would be a single point peak in the spectrum corresponding to the frequency of the carrier component as shown in fig 5.b. However when there is a short-term frequency variation within a burst, the spectrum obtained by FFT2 will not have a single point peak but a flat peak because the power of carrier component spreads in the frequency domain. Even this is the case; a smoothing of spectra employed in the first frequency estimation is still effective for second

frequency estimation to obtain a more accurate "average" frequency error involved after the first frequency error estimation. In this case, the window size must be smaller than the one in the first frequency estimation. It is noted that the estimated "average" frequency would not be utilized directly for the demodulation of signal because of the residual frequency variation of the second frequency estimator. To cope with this frequency variation, this paper proposes the novel phase synchronization method in Section
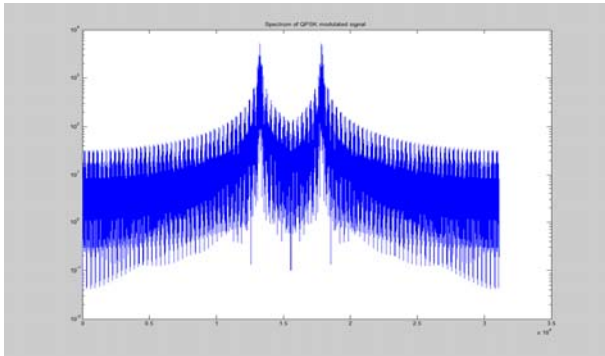
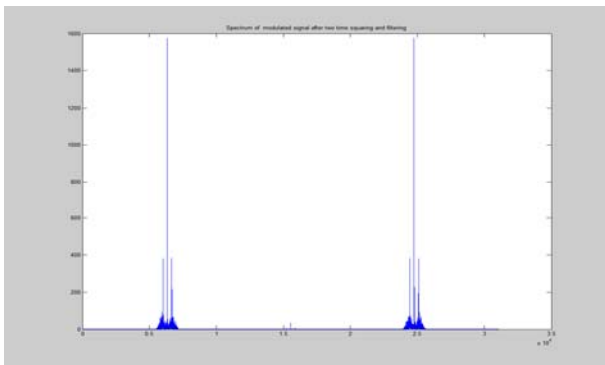Fig 5.a. QPSK Modulated signal spectrum

Fig 5.b. QPSK Modulated signal spectrum after squaring two times and filtering

C IFIR Heterodyning

Fig.6 gives the IFIR filter structure[4-7]. The function of IFIR technique is to convert digital pass band data to digital base band data by using digital frequency down conversion (DFDC) technique .In the I channel, alternate sample are passing through I(z) filter followed by decimation of 2 which will again filtered by 24 tap G(z) and further decimated by 2 to get baseband data samples in the output buffer.

Similarly for the Q channel. I(z) filter is Hilbert transform of I channel I(z) filter and G(z) filter is the same. The interpolating filter I(z) is half band filter and it is decimated by two to give I'(z). The IFIR technique greatly reduces the complexity of the design.
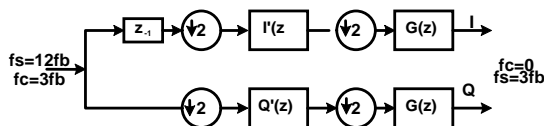

Fig 6   IFIR Filter Structure

D Digital Matched Filtering

The digital matched filtering is done on the samples at I and Q channel outputs. The digital matched filters operating on the base-band signal in case of QPSK are given by (k=0:8 for the 9 bits in I and Q streams, and σ =0:5 for the 6 timing offsets):

$$X_k(\sigma) = \sum_{m=(6k+\sigma)}^{(6k+\sigma+5)} x_m$$

$$Y_k(\sigma) = \sum_{m=(6k+\sigma)}^{(6k+\sigma+5)} y_m$$

where:

σ = timing offset and

x_m = output of I channel

y_m = output of Q channel

This matched filter uses rectangular weighting function and filtering is accomplished by accumulating the I and Q channel samples individually over the the duration of $2T_b$, where T_b =3.

Matched filtering is done on different NTIM timing offsets to address the issue of synchronization.

E UW Detector

Unique word sequence w_k should have good property of aperiodic autocorrelation defined as

$$C(\tau_{UW}) = \sum_{k=1}^{L_{UW}-\tau_{UW}} w_k w_{k+\tau_{UW}}^{*}$$

where L_{UW} is the unique word (UW) length in symbols and τ_{UW} is the delay between the received sequence and the correlator's sequence in the detector. The best sequence for this purpose is Barker sequence, with which it holds that $|C(\tau_{UW})|\leq 1$ for $\tau_{UW}\neq 0$. Binary and quaternary Barker sequences are shown in [8]. Maximal length of known binary and quaternary Barker sequences is 13. However, that value is too short to use for detecting frame of signals transmitted through satellite communications channel. Accordingly, we consider binary 16 bit sequence (3E4B) as UW sequence, which seems to have small aperiodic autocorrelation when τ_{UW} is restricted within small values. A QPSK FEC encoded UW detector was introduced in [9] (pp. 487), and its performance was analyzed in [10].

F Phase Estimation

Phase estimation is done using decision directed phase estimation[11-12]. The start phase is initially zero, and based on this the decision variables are computed over integration time of 36 bits per block. Then hard decision decoding is done on the decision variables computed using the start phase. The equations are as follows:

dvp1(σ)=x(σ)cos(strt_ph)+y(σ)sin(strt_ph)

dvp2(σ)=x(σ)cos(strt_ph)-y(σ)sin(strt_ph)

.Hard decision on dvp1(σ) and dvp2(σ) yields the I and Q channel bits i1(σ) and q1(σ) , which are used to estimate the phase using the following equations:

$Im\_sum_k = i1(\sigma)\ dvp2(\sigma) - q1(\sigma)\ dvp1(\sigma)$

$Re\_sum_k = i1(\sigma)\ dvp1(\sigma) + q1(\sigma)\ dvp2(\sigma)$

The carrier phase of each timing are estimated using:

$ph\_est(\sigma) = atan2\ (Im\_sum_k, Re\_sum_k)$

This phase estimate is used to form the decision variables again and the procedure is repeated two more times to get a better estimate of the carrier phase. The signal presence detection is also done as follows:

$Isq(\sigma) = Rsq(\sigma)\ cos^2(\sigma) + Ssq(\sigma)\ sin^2(\sigma)$
$\qquad + 2RS(\sigma)\ cos(\sigma)sin(\sigma)$

$Qsq(\sigma) = Ssq(\sigma)\ cos^2(\sigma) + Rsq(\sigma)\ sin^2(\sigma)$
$\qquad - 2RS(\sigma)\ cos(\sigma)sin(\sigma)$

where:

$Rsq(\sigma) = \sum_k x_k(\sigma)^2$

$Ssq(\sigma) = \sum_k y_k(\sigma)^2$

$RS(\sigma) = \sum_k x_k(\sigma)\ y_k(\sigma)$

The signal is said to be present if $|Qsq(\sigma)\ /\ Isq\ (\sigma)\ | < 1.5$ else the signal is not present. In QPSK , there is phase ambiguity of $\pm 90°$ and this problem is avoided in the phase estimation loop as the start phase gives a rough estimate of the next phase.
Such 6 timing offsets are calculated and the maximum of them is chosen to detect the signal. The present phase estimate is also stored here to be used for next block.

G. Coherent Detection
The final decision variables are obtained using the following equation:

$dv1 = x(\sigma)\ cos(\sigma_0) + y(\sigma)\ sin(\sigma_0)$

$dv2 = x(\sigma)\ cos(\sigma_0) - y(\sigma)\ sin(\sigma_0)$

The hard decision decoding is done by decoding these decision variables to obtain 2 bits at a time. If this variable is greater than 0 the data bit is a '1', otherwise it is '0'.

H. Differential Decoder and FEC decoding
The data bits obtained at the output of the coherent detection are differentially decoded through the differential decoder of the form

$Ak = [(\sim(ibit_k \oplus qbit_k))(\ ibit_k \oplus ibit_{k-1})$
$\qquad + (ibit_k \oplus qbit_k)(\ qbit_k \oplus qbit_{k-1})]$

$Bk = [(\sim(ibit_k \oplus qbit_k))(\ qbit_k \oplus qbit_{k-1})$
$\qquad + (ibit_k \oplus qbit_k)(\ ibit_k \oplus ibit_{k-1})]$

where ibit and qbit are the detected bits which are finally outputted as the demodulated data. The Differentially decoded date then pass through a Viterbi decoder chip,which is already configured in k=7,rate ½ mode in order to get a FEC decoded data.

VI. HARDWARE DESIGN
Fig 7. shows the realized Preambless QPSK based Burst demodulator, which can be used as signaling channel .
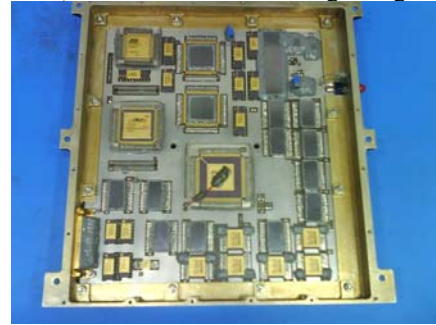

Fig 7.   Space Qualified QPSK based Burst demodulator

VII. TEST RESULTS:
Figure 8 shows the phase plot of the demodulator. The phase is obtained at the end of each block.
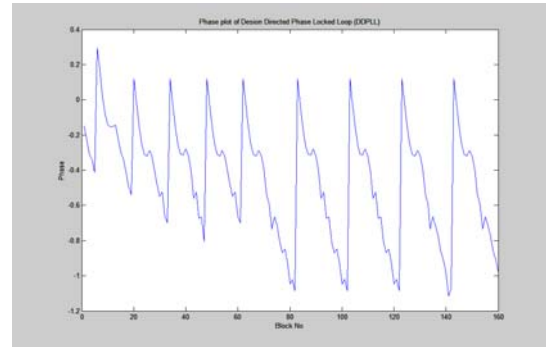

Fig. 8 Phase Curve

The BER curve of the DSP demodulator in comparison with the ideal curve is shown in Figure 9. Thus, the demodulator works with the implementation margin of 1 dB.
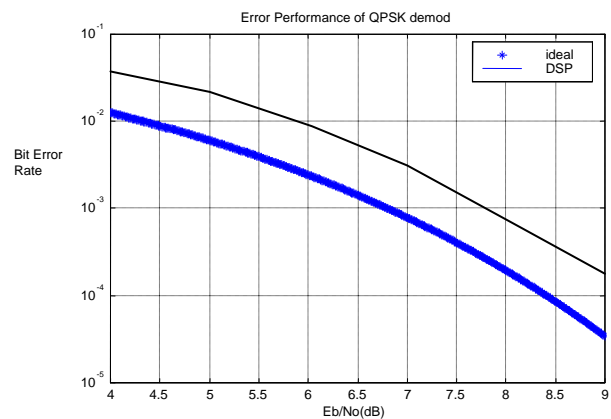

Fig. 9 BER curve

The following relation used to calculate the BER from PER (packet error rate) with assumption of uniform distribution of errors in data.

$$BER = [1 - (1-PER)^{1/PL}]$$

Where   PL : Packet length.

PER : Packet error rate

VIII. CONCLUSION

The 2.048 Mbps QPSK ½ Preambless demodulator implemented on ADSP-21020 platform using digital signal processing techniques meets the performance standards. It can be used for faster access in various satellite applications.

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